

REMARKS

The claims are claims 1 to 4, 7 to 10, 13 to 16 and 18 to 25.

Claims 1, 2, 7, 8, 13, 14 and 25 have been amended. Claims 5, 11 and 17 are canceled. Claims 1, 7 and 13 have been amended to incorporate subject matter of respective claims 5, 11 and 17. Claims 1, 7 and 13 include additional amendments distinguishing over the cited references. Claims 2, 8, 14 and 25 have been amended to distinguish over the cited references.

A copy of sheet 3 of the drawings including amended Figure 4 is attached. Figure 4 has been amended to include a line from the "NO" output of step 412 to the input of step 402. The specification has been amended at the paragraph bridging pages 12 and 13 to describe this connection.

Claims 1, 5, 7, 11, 13, 17, 24 and 25 were rejected under 35 U.S.C. 102(e) as anticipated by Herring U.S. Patent No. 6,606,326.

Claim 1 recites subject matter not anticipated by Herring. Claim 1 recites "not storing data read from said source port in intermediate buffers" "if said destination port is not capable of receiving data of said predetermined size." The FINAL REJECTION cites the paragraph bridging columns 3 and 4 of Herring as anticipating the operations "if the destination port is not capable of receiving data of the predetermined size." This portion of Herring states each input port includes a FIFO buffer and that these hold a queue of incoming messages. This portion of Herring teaches that these FIFO queues stall when the destination port cannot receive data. This is contrary to the recitations of claim 1, which recite that no such intermediate buffers store data when the destination port cannot receive data. Accordingly, claim 1 is allowable over Herring.

Claims 1, 7 and 13 recite subject matter not anticipated by Herring. Claims 1, 7 and 13 recite "if said destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said data transfer request." The FINAL REJECTION cites the paragraph bridging columns 3 and 4 of Herring as anticipating the operations "if the destination port is not capable of receiving data of the predetermined size." This portion of Herring states each input port includes a FIFO buffer and that these hold a queue of incoming messages. This portion of Herring teaches that these FIFO queues stall when the destination port cannot receive data. The Applicant respectfully submits that data stored in these FIFO buffers must have been read from the source port into the FIFO buffers. Accordingly, Herring fails to teach this limitation of not reading the source port if the destination port cannot receive data. The prohibition on reading the data from the source port if the destination port cannot receive the data of claims 1, 7 and 13, prevents data from being stalled in FIFO buffers in the path between source port and destination port. Accordingly, claims 1, 7 and 13 are allowable over Herring.

Claims 1, 7 and 13 recite further subject matter not anticipated by Herring. The FINAL REJECTION cites Herring at column 4, lines 38 to 49 as anticipating the recitations of prior claims 5, 11 and 17 (now incorporated into respective independent claims 1, 7 and 13). Claim 1 recites "if a second data transfer request is pending querying said second destination port to determine if said second destination port is capable of receiving data of said predetermined size, if said second destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said second data transfer request, not storing data read from said source port in intermediate buffers and

not transferring data to said second destination port thereby not blocking reading data from said source port until said second destination port is capable of receiving data." Claims 7 and 13 similarly recite "if a second data transfer request is pending querying said second destination port to determine if said second destination port is capable of receiving data of said predetermined size, if said second destination port is not capable of receiving data of said predetermined size, waiting by not reading data of said predetermined size from said source port corresponding to said second data transfer request thereby not blocking reading data from said source port until said second destination port is capable of receiving data." The cited portion of Herring teaches routing later messages in an input queue around the message at the head of the queue if that head message is stalled. If this second message is stalled in an input queue, it must be stored in an intermediate buffer contrary to the recitations of claim 1. If this second message is stalled in an input queue, it must also have been read from the source port contrary to the recitations of claims 1, 7 and 13. Accordingly, claims 1, 7 and 13 are allowable over Herring.

Claim 24 recites subject matter not anticipated by Herring. Claim 24 recites "said plurality of data processors, said request queue controller, said data transfer hub and said plurality of ports are disposed on a single integrated circuit." The FINAL REJECTION cites Figure 3 of Herring as anticipating this subject matter. The Applicant respectfully submits that Herring fails to teach that the circuit of Figure 3 is disposed on a single integrated circuit. The FINAL REJECTION does not cite any portion of Herring as teaching this single integrated circuit limitation. Herring states at column 5, lines 40 to 42:

"In essence, this packet switch relies on using a number of inter-connected single chip integrated circuit 8-by-8 time divisional uni-directional packet routers."

This portion of Herring teaches and 8-by-8 time divisional uni-directional packet router on a single integrated circuit. This fails to teach that plural data processors and a request queue controller are also disposed on this single integrated circuit. Accordingly, claim 24 is not anticipated by Herring.

Claim 25 recites subject matter not anticipated by Herring. Claim 25 recites the data transfer hub "controlling said source port and said destination port to not query said internal memory port to determine if said destination port is capable of receiving data of a predetermined size, read data of said predetermined size from said source port and transfer said read data to said destination port via said data transfer hub if said internal memory port is a destination port of a data transfer request." The FINAL REJECTION cites column 7, line 55 to column 8, line 6 of Herring as anticipating this limitation. Herring states at column 7, line 62 to column 8, line 6:

"The data packet control circuitry is adapted to forward a sequence of multiple portions of the data packet from the at least one input port to the at least one output port through the central queue path, and to identify during the forwarding a next portion of the multiple portions of the sequence as a critical portion to the at least one output port, and in response thereto, to switch forwarding of the sequence of multiple portions of the data packet from the central queue path to the bypass path so that the critical portion is passed directly from the at least one input port to the at least one output port through the bypass path irrespective of whether contention exists for the at least one output port."

This portion of Herring teaches using a bypass path, while claim 25 does not require such a bypass path but uses the normal path through the hub. This portion of Herring teaches use of the bypass path is based upon whether the message is "a critical portion." In contrast, the contingency recited in claim 25 is whether the

destination port is the internal memory port. Thus this portion of Herring teaches use of a different technique based upon a different contingency than recited in claim 25. Accordingly, claim 25 is allowable over Herring.

Claims 2 to 4, 8 to 10 and 14 to 16 are allowable by dependency upon allowable base claims.

Claims 19 to 23 have been ruled allowable.

The Applicant respectfully requests entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,



Robert D. Marshall, Jr.
Reg. No. 28,527